Amendments to the claims:

1. (Currently Amended) A method of delaying the counting of a number of occurrences of each of a plurality of events occurring in a processor complex having at least one processor until the disposition of an event has been determined, comprising the steps of:

providing at least one array of memory storage for storing count information for each of the plurality of events;

providing a plurality of separately addressable groups of memory addresses in each of the at least one array of memory storage;

providing at least one counter associated with each array of memory storage;

said at least one processor generating a plurality of counter parameters for each of the plurality of events, said counter parameters uniquely identifying each of the plurality of events, specifying a counter operation, and specifying one of the at least one counter for the operation;

providing a means for altering the disposition of an event, said means enabled to modify said parameters;

disposing a first event with the means for altering to create a first event disposition; ~~and~~

the means for altering modifying or not modifying the parameters responsive to the first event disposition; and

subsequently selecting an at least one counter and performing a counter operation on the selected counter responsive to the parameters.

2. (Original) The invention of claim 1, further comprising the steps of:

passing the parameters of each of the plurality of events generated by said at least one processor to at least one temporary buffer; and

the means for altering retrieving the parameters from the at least one temporary buffer.

3. (Original) The invention of claim 1 wherein the step of disposing the first event comprises forwarding the first event according to the parameters generated by the at least one processor, and wherein the step of modifying or not modifying the parameters comprises the step of not modifying the parameters.

4. (Original) The invention of claim 1 wherein the step of disposing the first event comprises the step of discarding the first event, and the wherein the step of modifying or not modifying the parameters comprises the step of modifying the parameters, said modification resulting in a change of destination for the counter operation to a different counter with respect to the counter specified by the parameters prior to their modification

5. (Original) The invention of claim 4, further comprising the step of the means for altering the disposition of an event performing a read modify write sequence on the different counter.

6. (Original) The invention of claim 4 wherein the means for altering the disposition of an event comprises at least one flow control algorithm, and the first event is discarded according to the algorithm.

7. (Original) The invention of claim 4 further comprising the steps of:

providing a queue for holding said events, said queue having a maximum capacity for holding events; and

enqueueing said events in said queue;

and wherein the step of disposing said event comprises the step of discarding the event, said discarding step responsive to the queue containing more events than said maximum capacity.

8. (Original) The invention of claim 4, further comprising the steps of:

providing a table which contains information including a point of reference in each array to uniquely define the structure and location of each array of memory; and providing a counter manager communicating with said at least one processor and said memory arrays and said means for altering the disposition of an event; and

wherein the step of performing a write operation further comprises the steps of:

passing the parameters from the means for altering to said counter manager after the step of modifying or not modifying the parameters; and

said counter manager, utilizing said table and said parameters of information from said at least one processor, determining the unique physical address location associated with the first event, reading the data from said determined address, modifying the read data and writing the modified data to the said determined addresses.

9. (Original) The invention of claim 8, wherein one of said parameters for each event includes a counter definition table index that identifies the counter definition entry to be used for a particular action.

10. (Original) The invention of claim 9 wherein one of said parameters for each of said events is a counter index and wherein there are a plurality of counters associated with each counter definition entry.

11. (Original) The invention as defined in claim 8 further characterized by said parameters including a counterset index, the number of counters per set and the counter number to be used for a particular address.

12. (Currently Amended) A structure for delaying the counting of a number of occurrences of each of a plurality of events occurring in a processor complex having at least one processor until the disposition of the event has been determined, comprising:

at least one array of memory storage for storing count information for each event in circuit communication with said at least one processor;

a plurality of separately addressable groups of memory addresses in each of the at least one array of memory;

at least one counter associated with each array of memory;

a plurality of parameters generated by said at least one processor for each of said events, said counter parameters uniquely identifying each said event, specifying a counter operation, and specifying one of the counters for the operation; ~~and~~

a means for altering the disposition of an event connected in circuit communication with said counters, said means enabled to modify said parameters~~;~~

wherein said means is configured to dispose a first event, retrieve the parameters, and decide to modify or not modify the parameters responsive to a disposition of the first event where the disposition indicates whether modification is required; and

a counter means configured to subsequently select an at least one counter and perform a counter operation on the selected counter responsive to the parameters.

13. (Original) The structure of claim 12 further comprising at least one temporary buffer connected to the at least one processor and the means for altering the disposition of an event and configured to receive the parameters from the at least one processor, wherein the means is configured to retrieve the parameters from the at least one temporary buffer.

14. (Original) The structure of claim 12 wherein the means is configured to dispose the first event by forwarding it according to the parameters generated by the at least one processor and responsively not modify the parameters.

15. (Original) The structure of claim 12 wherein the means is configured to dispose the first event by discarding the event and responsively modify the parameters.

16. (Original) The structure of claim 15 wherein the means is configured to responsively perform a read modify write sequence on the different counter.

17. (Original) The invention of claim 15 wherein the means comprises at least one flow control algorithm, and the first event is discarded according to the algorithm.

18. (Original) The invention of claim 15, further comprising a queue for holding said events, said queue having a maximum capacity for holding events, wherein the events are enqueued said in said queue and wherein the first event is discarded responsive to the queue containing more events than said maximum capacity.

19. (Original) The invention of claim 15, further comprising:

a table which contains information including a point of reference in each array to uniquely define the structure and location of each array of memory; and

a counter manager communicating with said at least one processor and said memory arrays and said means for altering the disposition of an event;

wherein the counter manager is configured to receive the parameters from the means after the means has modified or not modified the parameters; and

said counter manager, utilizing said table and said parameters of information from said at least one processor, is configured to determine the unique physical address location associated with said first event, read the data from said determined address, modify the read data and write the modified data to the determined addresses.

20. (Original) The invention of claim 19, wherein one of said parameters for each event includes a counter definition table index that identifies the counter definition entry to be used for a particular action.

21. (Original) The invention of claim 20 wherein one of said parameters for each of said events is a counter index and wherein there are a plurality of counters associated with each counter definition entry.

22. (Original) The invention as defined in claim 19 wherein said parameters further comprise a counterset index, the number of counters per set, and the counter number to be used for a particular address.